

In the claims:

For the Examiner's convenience, all pending claims are presented below with changes shown in accordance with the mandatory amendment format.

1 1. (Currently Amended) A chipset comprising:
2 a graphics accelerator;
3 a memory controller; and
4 a queue mechanism divided to include~~including~~:
5 a first functional unit block (FUB)₁ coupled to the graphics accelerator, to
6 perform a first set of functions for the queue mechanism; and
7 a second FUB₂ coupled to the memory controller, to perform a second set
8 of functions for the queue mechanism.

1 2. (Original) The chipset of claim 1 wherein the queue mechanism further
2 comprises control logic to facilitate an interface between the graphics accelerator and the
3 memory controller.

1 3. (Original) The chipset of claim 1 wherein the first FUB is operated based
2 upon a first clock domain and the second FUB is operated according to a second
3 clock domain.

1 4. (Original) The chipset of claim 1 wherein there is unidirectional signaling
2 between the first FUB and the second FUB, such that there will be a strobe and a
3 packet associated with the strobe that flows from the first FUB to the second FUB.

1 5. (Original) The chipset of claim 3 wherein the second FUB comprises
2 storage elements in which to store information that is written into the queue
3 mechanism.

1 6. (Original) The chipset of claim 5 wherein the first FUB comprises:
2 logic associated with a load pointer, wherein the load pointer indicates a
3 location in the storage elements to store information; and
4 match logic.

1 7. (Original) The chipset of claim 6 wherein the second FUB comprises:
2 an unload pointer to indicate a location in the storage elements in which
3 information is to be read from; and
4 clock gating elements to gate the load pointer into the second clock domain.

1 8. (Original) The chipset of claim 7 wherein the match logic compares the load
2 and unload pointer to determine whether information is stored in the queue.

1 9. (Original) The chipset of claim 8 wherein the load pointer is clock crossed to
2 the second clock domain in FUB 1 to save a clock of latency.

1 10. (Original) The chipset of claim 9 wherein the unload pointer is clock crossed
2 to the first clock domain in the second FUB.

1 11. (Original) The chipset of claim 10 wherein data to be stored in the storage
2 elements is directly flopped in the first clock domain within the second FUB.

1 12. (Original) The chipset of claim 10 wherein the clock crossed versions of the
2 load pointer and the unload pointer are used to determine at the second FUB if a
3 command is present.

1 13. (Original) The chipset of claim 12 wherein the availability of space in the
2 storage elements is determined at the match logic by using the load pointer and the clock
3 crossed version of the unload pointer.

1 14. (Currently Amended) A system comprising:
2 a first component;
3 a second component; and
4 a queue mechanism divided to include including:
5 a first functional unit block (FUB)₁ coupled to the first component, to
6 perform a first set of functions for the queue mechanism; and
7 a second FUB₂ coupled to the second component, to perform a second set
8 of functions for the queue mechanism.

1 15. (Original) The system of claim 14 wherein the first FUB is operated based
2 upon a first clock domain and the second FUB is operated according to a second
3 clock domain.

1 16. (Original) The system of claim 15 wherein the second FUB comprises
2 storage elements in which to store information that is written into the queue
3 mechanism.

1 17. (Original) The system of claim 16 wherein the first FUB comprises:
2 logic associated with a load pointer, wherein the load pointer indicates a
3 location in the storage elements to store information; and
4 match logic.

1 18. (Original) The system of claim 17 wherein the second FUB comprises:
2 an unload pointer to indicate a location in the storage elements in which
3 information is to be read from; and
4 clock gating elements to gate the load pointer into the second clock domain.

1 19. (Currently Amended) A queue mechanism comprising:
2 a first functional unit block (FUB)₁ coupled to a first component, to perform a first
3 set of functions for the queue mechanism; and
4 a second FUB₂ coupled to a second component, to perform a second set of
5 functions for the queue mechanism.
6 control logic to facilitate an interface between the first component and the second
7 component.

1 20. (Original) The queue mechanism of claim 19 wherein the first FUB is
2 operated based upon a first clock domain and the second FUB is operated according
3 to a second clock domain.

1 21. (Original) The queue mechanism of claim 20 wherein the second FUB
2 comprises storage elements in which to store information that is written into the
3 queue mechanism.

1 22. (Original) The queue mechanism of claim 21 wherein the first FUB
2 comprises:
3 logic associated with a load pointer, wherein the load pointer indicates a
4 location in the storage elements to store information; and
5 match logic.

1 23. (Original) The queue mechanism of claim 22 wherein the second FUB
2 comprises:
3 an unload pointer to indicate a location in the storage elements in which
4 information is to be read from; and
5 clock gating elements to gate the load pointer into the second clock domain.

1 24. (Original) The queue mechanism of claim 23 wherein the match logic
2 compares the load and unload pointer to determine whether information is stored in the
3 queue.

- 1 25. (Original) The queue mechanism of claim 24 wherein the load pointer is
2 clock crossed to the second clock domain in FUB 1 to save a clock of latency.
- 1 26. (Original) The queue mechanism of claim 25 wherein the unload pointer is
2 clock crossed to the first clock domain in the second FUB.
- 1 27. (Original) The queue mechanism of claim 26 wherein data to be stored in the
2 storage elements is directly flopped in the first clock domain within the second FUB.
- 1 28. (Original) The queue mechanism of claim 26 wherein the clock crossed
2 versions of the load pointer and the unload pointer are used to determine at the second
3 FUB if a command is present.
- 1 29. (Currently Amended) The queue mechanism ~~chipset~~ of claim 28 wherein the
2 availability of space in the storage elements is determined at the match logic by using the
3 load pointer and the clock crossed version of the unload pointer.
- 1 30. (Currently Amended) A computer system comprising:
2 a memory control hub (MCH) having:
3 a graphics accelerator;
4 a memory controller;
5 a queue mechanism divided to include ~~including~~:

6 a first functional unit block (FUB)₁ coupled to the graphics
7 accelerator, to perform a first set of functions for the queue mechanism;
8 and
9 a second FUB₁ coupled to the memory controller, to perform a
10 second set of functions for the queue mechanism.

1 3031. (Currently Amended) The computer system of claim 30 wherein the queue
2 mechanism further comprises control logic to facilitate an interface between the graphics
3 accelerator and the memory controller.

1 3132. (Currently Amended) The computer system of claim 30 wherein the first FUB is
2 operated based upon a first clock domain and the second FUB is operated according
3 to a second clock domain.